TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6L08

Gate Driver for TFT LCD Panels

The T6L08 is a 240-channel-output gate driver for TFT LCD panels. In addition to high-voltage operation (liquid crystal drive voltage = max 42 V), this device accepts external input of the panel drive voltage, allowing you to change the low-level output voltage. Thus, this device can be used for various TFT LCD panel drive systems.
The T6L08 offers high integration circuit due to CMOS technology.

Unit: mm

T6L08	User Area Pitch	
	IN	OUT
(SAN, 3NS)	0.9	0.1
(SBN, 4DS)	0.9	0.1

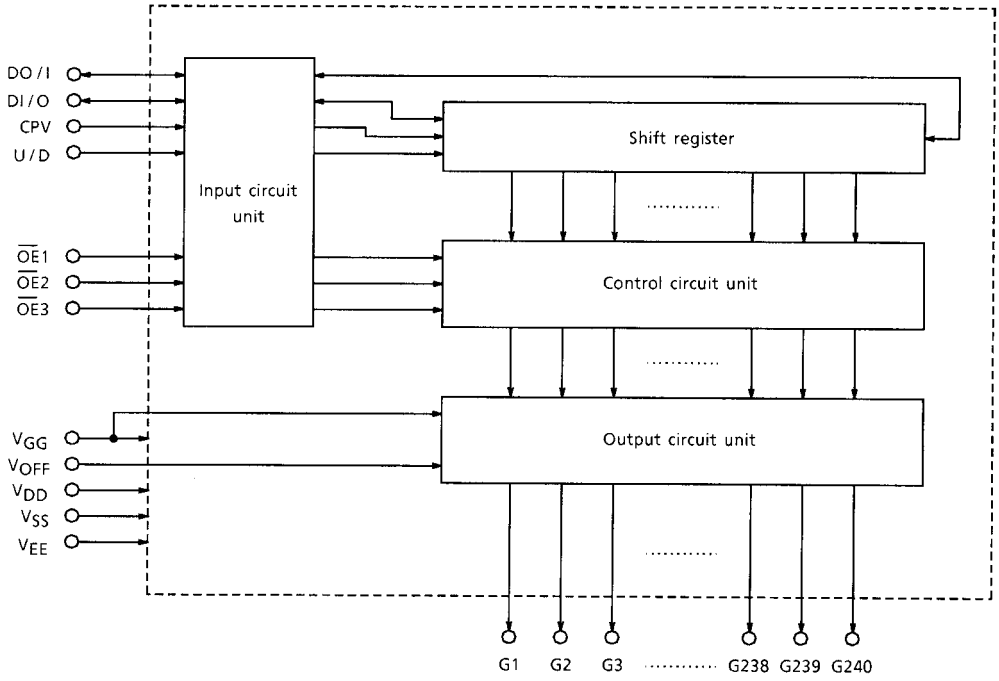
Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

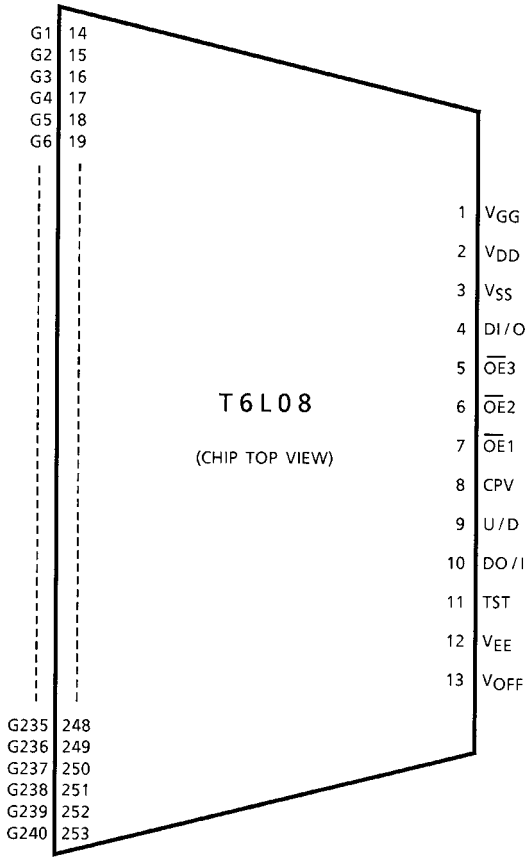
Features

- LCD drive output pins : 240 pins
- LCD drive voltage : Max V_{EE} + 42 V
- Data transfer method : Bidirectional shift register
- Operating temperature : −20 to 75°C
- Package : Tape carrier package (TCP)

Block Diagram



Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

Pin Function

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical shift data I/O pins.
These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below.
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
When set for input
This pin is used to feed data into the shift registers at the first stage of the LCD driver. The data is latched into the shift registers at the rising edge of CPV.
When set for output
When two or more T6L08s are cascaded, this pin outputs the data to be fed into the next stage. This data changes state synchronously with the falling edge of CPV.</td></tr>
<tr><td>U/D</td><td>Input</td><td>Transfer direction select pin
This pin specifies the direction in which data is transferred through the shift registers.
When U / D is high, data is shifted in the direction
G1 → G2 → G3 → G4 → G5 → ···→ G240
When U / D is low, the direction is reversed to give
G240 → G239 → G238 → G237 → ···→ G1
The voltage applied to this pin must be a DC−level voltage that is either high (V_{DD}) or low (V_{SS}).</td></tr>
<tr><td>CPV</td><td>Input</td><td>Vertical shift clock
This is the shift clock for the shift registers. Data is shifted through the shift registers synchronously with the rising edge of CPV.</td></tr>
<tr><td>$\overline{OE}$ 1 to $\overline{OE}$ 3</td><td>Input</td><td>Output enable input
These signals control the data appearing at the LCD panel drive pins (G1 to G240).
The V_{OFF} voltage is output when $\overline{OE}$ 1 to $\overline{OE}$ 3 are high; normal shift data is output when $\overline{OE}$ 1 to $\overline{OE}$ 3 are low.</td></tr>
<tr><td>V_{OFF}</td><td>Input</td><td>Analog input pin
If the shift register data is low (= logic 0), the voltage on this pin is forwarded to the output pin corresponding to the shift register. If $\overline{OE}$ 1 to $\overline{OE}$ 3 are high, the voltage on this pin is output irrespective of whether the shift register data is high or low.</td></tr>
<tr><td>TST</td><td>Input</td><td>Test pin
Leave this pin open.</td></tr>
<tr><td>G1 to G240</td><td>Output</td><td>LCD panel drive pins
These pins output the shift register data, or the voltage applied to V_{GG} or V_{OFF}, depending on the control signals $\overline{OE}$ 1 to $\overline{OE}$ 3.</td></tr>
<tr><td>V_{GG}</td><td>—</td><td>Power supply for LCD drive</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply for the internal logic</td></tr>
<tr><td>V_{SS}</td><td>—</td><td>Power supply for the internal logic</td></tr>
<tr><td>V_{EE}</td><td>—</td><td>Power supply for LCD drive and the internal logic</td></tr>
</table>

Device Operation (See Timing Diagram)

(1) Shift data transfer method

The input shift data is latched into the internal register synchronously with the rising edge of the shift clock CPV. When the data is shifted to the next register at the next rising edge of CPV, new input shift data is simultaneously latched into.
In the case of shift data output, the data in the last shift register is output synchronously with the falling edge of CPV (the output high voltage level is V_{DD}; the output low voltage level is V_{SS}).

U/D	DI/O	DO/I	Data Transfer Method
H	Input	Output	DI/ O → G1 → G2 → G3 → ·····→ G240 → DO/I
L	Output	Input	DO/I → G240 → G239 → G238 → ·····→ G1 → DI/O

(2) LCD panel drive outputs

If the shift register data corresponding to an output pin is high (= logic 1), the pin outputs V_{GG}; if the shift register data is low (= logic 0), the pin outputs V_{OFF}.
However, if $\overline{OE}$ 1 to $\overline{OE}$ 3 corresponding to the output pins are high, the pins output V_{OFF} irrespective of whether the shift register data is high or low. The LCD panel drive outputs are controlled by $\overline{OE}$ as shown below.

Output Enable Pin		Lcd Panel Drive Outputs	
H/L	$\overline{OE}$ 1 to 3	LCD Panel Drive Pins Controlled By $\overline{OE}$	Output
L	$\overline{OE}$ 1	G1, G4, G7, G10 ····· G235, G238	Normal data output
	$\overline{OE}$ 2	G2, G5, G8, G11 ····· G236, G239	
	$\overline{OE}$ 3	G3, G6, G9, G12 ····· G237, G240	
H	$\overline{OE}$ 1	G1, G4, G7, G10 ····· G235, G238	V_{OFF}
	$\overline{OE}$ 2	G2, G5, G8, G11 ····· G236, G239	
	$\overline{OE}$ 3	G3, G6, G9, G12 ····· G237, G240	

(3) Voltage setting

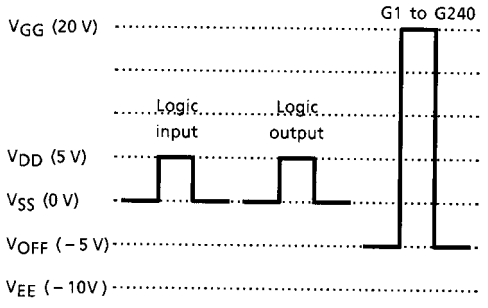
(Example 1) Negative voltage output

Logic input	: High = 5 V or low = 0 V amplitude
Supply voltage	: V_{GG} = 20 V
	V_{DD} = 5 V
	V_{OFF} = −5 V
	V_{EE} = −10 V
LCD panel drive output	: High level = V_{GG} (20 V)
	Low level = V_{GG} (−5 V)

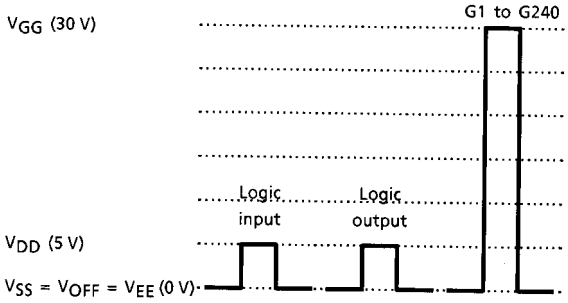
(Example 2) Positive voltage output

Logic input	: High = 5 V or low = 0 V amplitude
Supply voltage	: V_{GG} = 30 V
	V_{DD} = 5 V
	V_{OFF} = V_{SS} = V_{EE} = 0 V
LCD panel drive output	: High level = V_{GG} (30 V)
	Low level = V_{OFF} (0 V)

(*) Logic input pins : DI/O or DO/I, CPV, $\overline{OE}$1 to $\overline{OE}$3, U/D



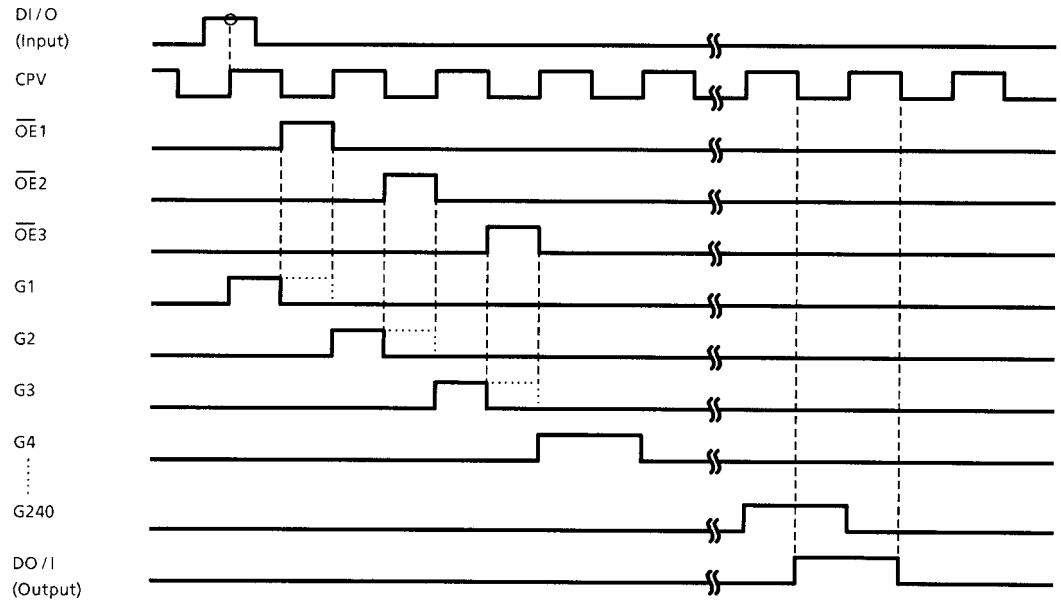
(Example 1)



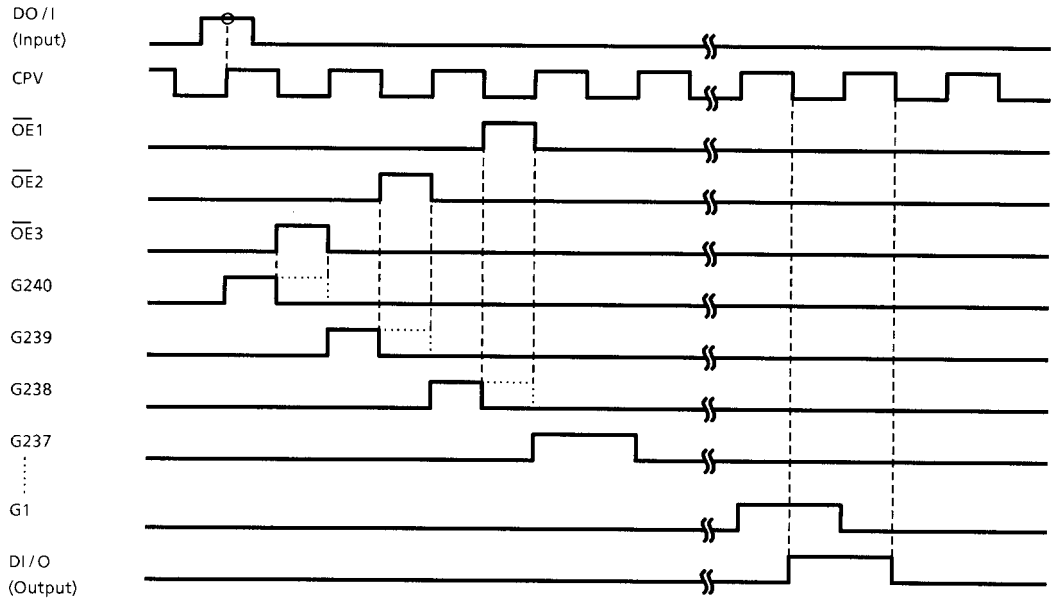
(Example 2)

Timing Diagrams

- **UP mode (U/D = high)**



- **DOWN mode (U/D = low)**



Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage (1)	$V_{GG} - V_{EE}$	15.0 to 45.0	V
Supply Voltage (2)	V_{DD}	−0.3 to 7.0	V
Supply Voltage (3)	V_{EE}	−16.0 to 0.3	V
Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Analog Input Voltage	V_{OFF}	V_{EE} − 0.3 to V_{GG} + 0.3	V
Storage Temperature	T_{STG}	−55 to 125	°C

Recommended Operating Conditions (V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage (1)	$V_{GG} - V_{EE}$	15.0 to 42.0	V
Supply Voltage (2)	V_{DD}	4.5 to 5.5	V
Supply Voltage (3)	V_{EE}	−15.0 to 0	V
Operating Temperature	T_{op}	−20 to 75	°C
Operating Frequency	F_{CPV}	DC to 100	kHz
Output Load Capacitance	C_L	300 (max)	pF / pin
Analog Input Voltage	V_{OFF} (Note 1)	−15.0 to 0	V

Note 1: $V_{EE} \leq V_{OFF}$

Electrical Characteristics

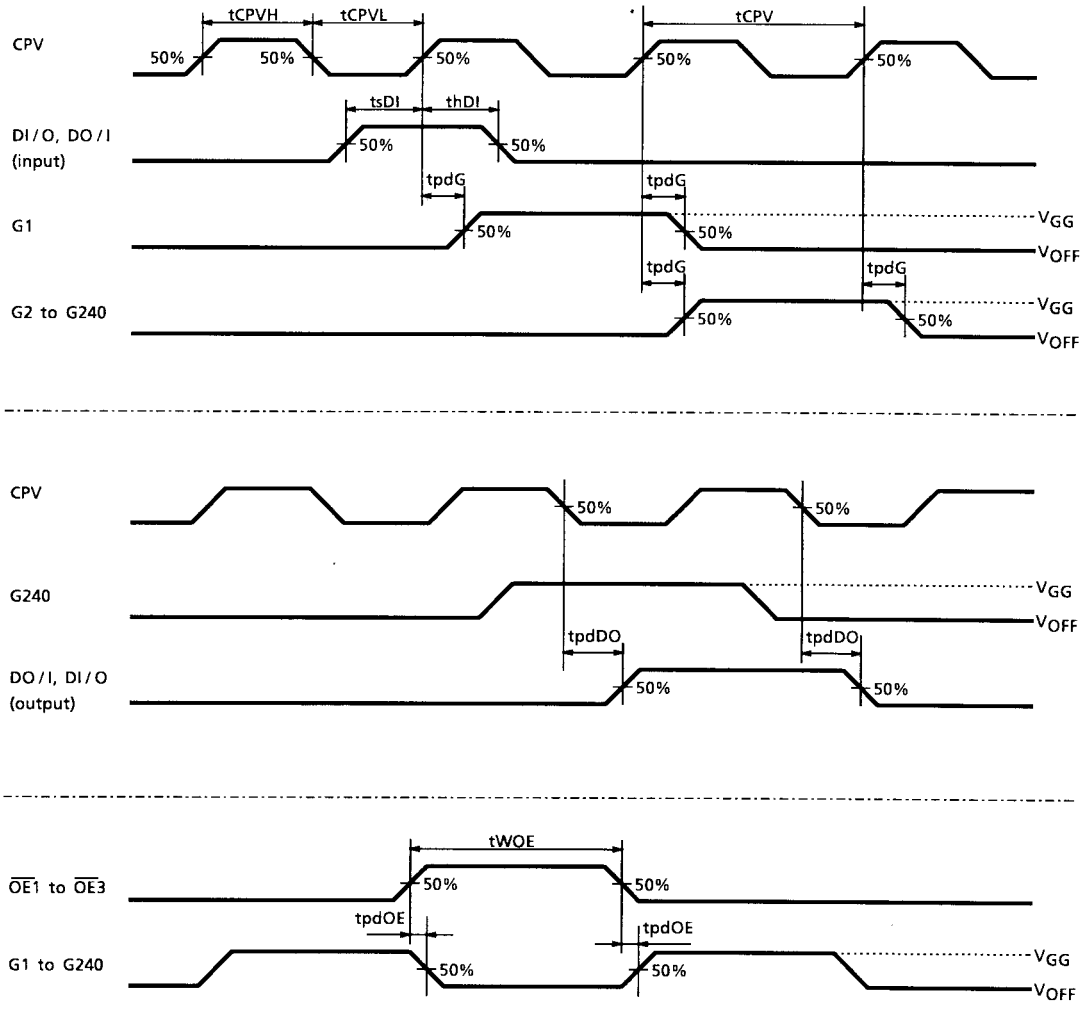
DC Characteristics (V_{GG} − V_{EE} = 42 V, Ta = −20 to 75°C)

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Relevant Pin
Input Voltage	Low Level	V_{IL}	—		V_{SS}	—	$0.2 \times (V_{DD} - V_{SS}) + V_{SS}$	V	(Note 2)
	High Level	V_{IH}			$0.8 \times (V_{DD} - V_{SS}) + V_{SS}$	—	V_{DD}		
Output Voltage	Low Level	V_{OL}	—	I_{OL} = 40 μA	V_{SS}	—	V_{SS} + 0.3 V	V	DI/O, DO/I
	High Level	V_{OH}		I_{OH} = −40 μA	V_{DD} − 0.3 V	—	V_{DD}		
Output Resistance	Low Level	R_{OL}	—	$V_{OUT} = V_{OFF}$ + 0.5 V	—	—	1500	Ω	G1 to G240
	High Level	R_{OH}		$V_{OUT} = V_{GG}$ − 0.5 V	—	—	1500		
Input Leakage Current		I_{IN}	—	—	−1.0	—	—	μA	(Note 2)
Current Consumption (1)		I_{GG}	—	—	—	—	—	μA	V_{GG}
Current Consumption (2)		I_{DD}	—	—	—	—	—	μA	V_{DD}
Current Consumption (3)		I_{SS}	—	—	−200	—	—	μA	V_{SS}

Note 2: Input pins include … DI/O, DO/I, U/D, CPV, $\overline{OE}$1 to $\overline{OE}$3

AC Characteristics (V_{GG} − V_{EE} = 42 V, Ta = −20 to 75°C)

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock Period	tCPV	—	—	10	—	—	μs
CPV Pulse Width (H)	tCPVH	—	—	4	—	—	μs
CPV Pulse Width (L)	tCPVL	—	—	4	—	—	μs
OE Enable Time	twOE	—	—	1	—	—	μs
Data Set−up Time	tsDI	—	—	1	—	—	μs
Data Hold Time	thDI	—	—	1	—	—	μs
Output Delay Time (1)	tpdDO	—	C_L = 50 pF	—	—	1	μs
Output Delay Time (2)	tpdG	—	C_L = 300 pF	—	—	1	μs
Output Delay Time (3)	tpdOE	—	C_L = 300 pF	—	—	1	μs


tCPVH
tCPVL
tCPV
CPV
50%
tsDI
thDI
DI / O, DO / I
(input)
tpdG
G1
VGG
VOFF
G2 to G240
CPV
G240
tpdDO
DO / I, DI / O
(output)
tWOE
OE1 to OE3
tpdOE
G1 to G240

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